UNITED STATES DEPARTMENT OF COMMERCE
Pat nt and Trademark Offic
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/256,643	02/23/99	FORBES L	303.324US2

021186 MMC2/0104
SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH
P.O. BOX 2938
MINNEAPOLIS MN 55402

EXAMINER	
TRINH, M	
ART UNIT	**PAPER NUMBER**
2822	14

DATE MAILED: 01/04/01

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trad marks

Office Action Summary	Application No. 09/256,643	Applicant(s) FORBES ET AL.	
	Examiner Michael M. Trinh	Art Unit 2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 October 2000* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *21,23,24,26,29-33 and 36-75* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *21,23,24,26,29-33 and 36-75* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. & 119(e).

Attachment(s)

15) ☒ Notice of References Cited (PTO-892)
16) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
17) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *12* .
18) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
19) ☐ Notice of Informal Patent Application (PTO-152)
20) ☐ Other: .

DETAILED ACTION

*** Amendment filed Oct 10, 2000 has been entered as paper number 13/C. , in which claims 34-35 were canceled, and in which claims 36-75 have been newly added. Claims 21, 23-24,26,29-33,36-75 are pending.

Claim Rejections - 35 USC § 112

1. Claims 60-75 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Re claims 60-64 and 68-72; claims 65-67 and 73-75: For example, between base claim 60 and 68, the claimed processing steps of base claim 60 and base claim 68 are *identical*. The only difference is in the preambles of claims 60 and 68. However, first, although claim 60 does not expressly mention "memory cell", the floating gate transistor is a form of memory cell. Second, although preamble of claim 68 recites "memory cell", it is still considered as a floating gate transistor since no additional limitation to make claim 68 being a "memory cell". Meaning and scope of the claims are unclear and indefinite. Similar discussion is to base claim 65 and 73, and other respective dependent claims.

Claim Rejections - 35 USC § 103

2. Claims 21,23-26,29-33,36-75 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamazaki et al (5,449,941) taken with Halvis et al (5,369,040).

Yamazaki et al teaches a method for forming a MOS transistor for memory cell (Figs 1A-1D; 2A-2D; col 4, lines 12-15; lines 27-60; col 3,lines 66-68) comprising: forming a source region and drain region in a semiconductor silicon substrate 101 (Fig 1D; col 4, lines 23-26), wherein a channel region being between the source and drain regions; forming an insulating layer 106 on the channel region; forming a floating gate 107 by patterning and etching a layer of gate material; forming a intergate dielectric layer 108; and forming a control gate 109 over the floating gate.

Yamazaki lack to form the floating gate of silicon carbide compound.

However, *Halvis* et al teach (at col 4, lines 10-15; cols 3-4), rather using polysilicon gate, using silicon carbide compound $Si_{1-x}C_x$, wherein x is selected at a value approximately between 0 and 0.5. for forming a gate on the gate insulating layer.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to replace the polysilicon gate of Yamazaki with the floating gate of silicon carbide compound $Si_{1-x}C_x$, wherein x is selected at a value approximately between 0 and 0.5 as taught by Halvis et al. This is because of the desirability to improve response, to improve quantum efficiency, and to improve performance and light sensitivity. Regarding other limitations including deposition techniques, for example, in claim 40, it would have been obvious to one of ordinary skill in the art to use any available and well known deposition techniques to deposit a silicon carbide compound on the gate insulating layer because these deposition techniques have been proven in the art to be able to effective form a reliable and excellent layer. Forming an oxide by dry plasma oxidation would have been obvious and well known to skill artisan because of the desirability to obtain a high quality and low defect oxide. Implanting dopant into the gate would have been obvious and well known to one of ordinary skill in the art because of the desirability to control conductivity of the gate.

The "person having ordinary skill" in this art has the capability of understanding the scientific and engineering principles applicable to the claimed invention. The evidence of record including the references and/or the admissions are considered to reasonably reflect this level of skill. The selection of x value would have been obvious, involve routine optimization which has been held to be within the level of ordinary skill in the art, and would be an unpatentable modification, where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation". *In Re Aller* 104 USPQ 233,255 (CCPA 1955); *In re Waite* 77 USPQ 586 (CCPA 1948) and *In Re Dreyfus* 24 USPQ 52 (CCPA 1934).

3. Claims 43-45,48-512,55-57,60-61,65-66,68-69,71-74 are rejected under 35 U.S.C. 103(a) as being unpatentable over Halvis et al (5,369,040) taken with Tohyama (5,858,811).

Halvis et al teaches a method for forming a semiconductor device (Figs 4A-4C; cols 3-4) comprising: forming an insulating layer 32 on the channel region; forming a floating gate 38 by

patterning and etching a layer of gate material 33 (figs 4A-4B; col 3, line 61 through col 4); forming a intergate dielectric layer 42 by oxidizing; and forming a control gate 50 over the floating gate 38 with the intergate dielectric layers 42 therebetween (Fig 4C).

Halvis lack to remove portion of the insulating layer during formation of the gate 38.

However, *Tohyama* et al alternatively teach (at Fig 1 to 4; col 1-3, cols 5-6) either removing portions of the first insulating layer 4 (Fig 3C; col 2, lines 40-63) and the layer of gate material 6 to form a gate 8, or not removing a portion of the first insulating layer 4 (Figs 1C-1D); forming an interlayer dielectric layer; and forming a second gate 13, wherein the gate layer is doped with n-type or p-type impurities (col 6, lines 20-25)

It would have been obvious to one of ordinary skill in the art at the time the invention was made to remove portions of the insulating layer and the layer of silicon carbide of Halvis in forming the gate as taught by Tohyama. This is because of the desirability to control the desired thickness of the gate insulating layer, wherein thickness of each of the gate insulating layers are formed independently from each other.

Regarding other limitations including deposition techniques, for example, in claim 44, it would have been obvious to one of ordinary skill in the art to use any available and well known deposition techniques to deposit a silicon carbide compound on the gate insulating layer because these deposition techniques have been proven in the art to be able to effective form a reliable and excellent layer. Forming an oxide by dry plasma oxidation would have been obvious and well known to skill artisan because of the desirability to obtain a high quality and low defect oxide. Implanting n-type or p-type dopants into the gate would have been obvious and well known to one of ordinary skill in the art because of the desirability to control conductivity of the gate.

The "person having ordinary skill" in this art has the capability of understanding the scientific and engineering principles applicable to the claimed invention. The evidence of record including the references and/or the admissions are considered to reasonably reflect this level of skill. The selection of x value would have been obvious, involve routine optimization which has been held to be within the level of ordinary skill in the art, and would be an unpatentable modification, where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation". *In Re Aller*

104 USPQ 233,255 (CCPA 1955); *In re Waite* 77 USPQ 586 (CCPA 1948) and *In Re Dreyfus* 24 USPQ 52 (CCPA 1934).

Response to Arguments

*** Applicant's convincing remarks that the present divisional application has the same filing date of July 29, 1997 as that of Forbes 5,886,368. The rejection using Forbes reference is withdrawn.

4. Applicant's other arguments filed Oct 10, 2000 have been fully considered but they are not persuasive, and to are also moot in view of the new ground(s) of rejection.

** Regarding 35 USC 112 rejection of claims 60-75:

** In response to applicant's arguments about 35 USC 112 rejection, the recitation "transistor" or "memory cell" has not been given patentable weight because the recitation occurs in the preamble. A preamble is generally not accorded any patentable weight where it merely recites the purpose of a process or the intended use of a structure, and where the body of the claim does not depend on the preamble for completeness but, instead, the process steps or structural limitations are able to stand alone. See *In re Hirao*, 535 F.2d 67, 190 USPQ 15 (CCPA 1976) and *Kropa v. Robie*, 187 F.2d 150, 152, 88 USPQ 478, 481 (CCPA 1951). A recitation of the intended use of the claimed invention must result in a structural difference. In a claim drawn to a process of making, the intended use must result in a manipulative difference. See *In re Casey*, 152 USPQ 235 (CCPA 1967) and *In re Otto*, 136 USPQ 458, 459 (CCPA 1963).

In this instant case, for example, between base claim 60 and 68, the claimed processing steps of base claim 60 and base claim 68 are *identical*, in which the body of each claim does not depend on the preamble for completeness but, instead, the process steps or structural limitations are able to stand alone. The claimed inventions of claims 60 and 68 do not result in a structural difference or a processing difference. Therefore, further limitations should be expressly included in claim 68 so as to distinguish claim 68 as a "memory cell" from a "transistor" as claimed in claim 60. Similar discussion is to base claim 65 and 73, and other respective dependent claims.

** Regarding Art rejection:

** Applicant remarks (at remark, page 11 filed 10/10/00) that "...Halvis does not disclose forming a source region and a drain region...". This is noted and found unconvincing. First, this is a 35 USC 103 rejection, in which the main reference of Yamazaki clearly teaches to form source region 103 and drain region 104. Second, as can be seen, claims 43,50,55,60,65,68,73 do not recite "forming a source region and a drain region...". That limitation(s) is not found in the claims. Claimed subject matter, not the specification, is the measure of invention. Limitations in the specification cannot be read into the claims for the purpose of avoiding the prior art. In Re Self, 213 USPQ 1,5 (CCPA 1982); In Re Priest, 199 USPQ 11,15 (CCPA 1978).

** Applicant remarks about Yamazaki and Halvis that "...structures are very different and operate in a different manner..." are noted and found unconvincing. Structure and operation of the gate of both devices are substantially the same. Replacing different materials in forming the gate would have been obvious to skill artisan. It would have been obvious to one of ordinary skill in the art at the time the invention was made to replace the polysilicon gate of Yamazaki with the floating gate of silicon carbide compound $Si_{1-x}C_x$, as taught by Halvis et al. This is because of the desirability to improve response, to improve quantum efficiency, and to improve performance and light sensitivity.

** Applicant further remarks (remark, page 11, third paragraph) that "...Yamazaki discloses a memory cell with a source region 203, a drain region 204, a floating gate 208, and a control gate 210...Therefore, one skilled in the art would not have been motivated to form either the floating gate 107 or the control gate 109 shown in Figure 1D from the same material as the insulator 105". This is noted and found unconvincing. By forming the floating gate 208, as also shown in Figures 2D of Yamazaki, using the silicon carbide compound, $Si_{1-x}C_x$, as obviously taught by Halvis et al, the modified floating $Si_{1-x}C_x$ gate 208 is not the same material as the silicon oxide insulator 207 (col 3, lines 37-68).

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Regarding "...structures are very different and operate in a different manner...", Kooi et al (4113,515) evidently teach his method is obviously applicable in fabrication of both a

photodetector charge transfer device having a gate 7(figs 1-3; col 5), and a MOS device having a gate 93, source region and drain region (Figs 8-12; col 8, lines 31-68).

****

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

****

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael M. Trinh9 whose telephone number is (703) 308-2554. The examiner can normally be reached on M-F from 8:30 Am to 4:30 Pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Whitehead Jr Carl can be reached on (703) 308-4940. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-1782.
Oasc

Michael Trinh
Primary Examiner